

Bhakta, et al.

Atty Docket: NETL.001DV2

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ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY
MODULE

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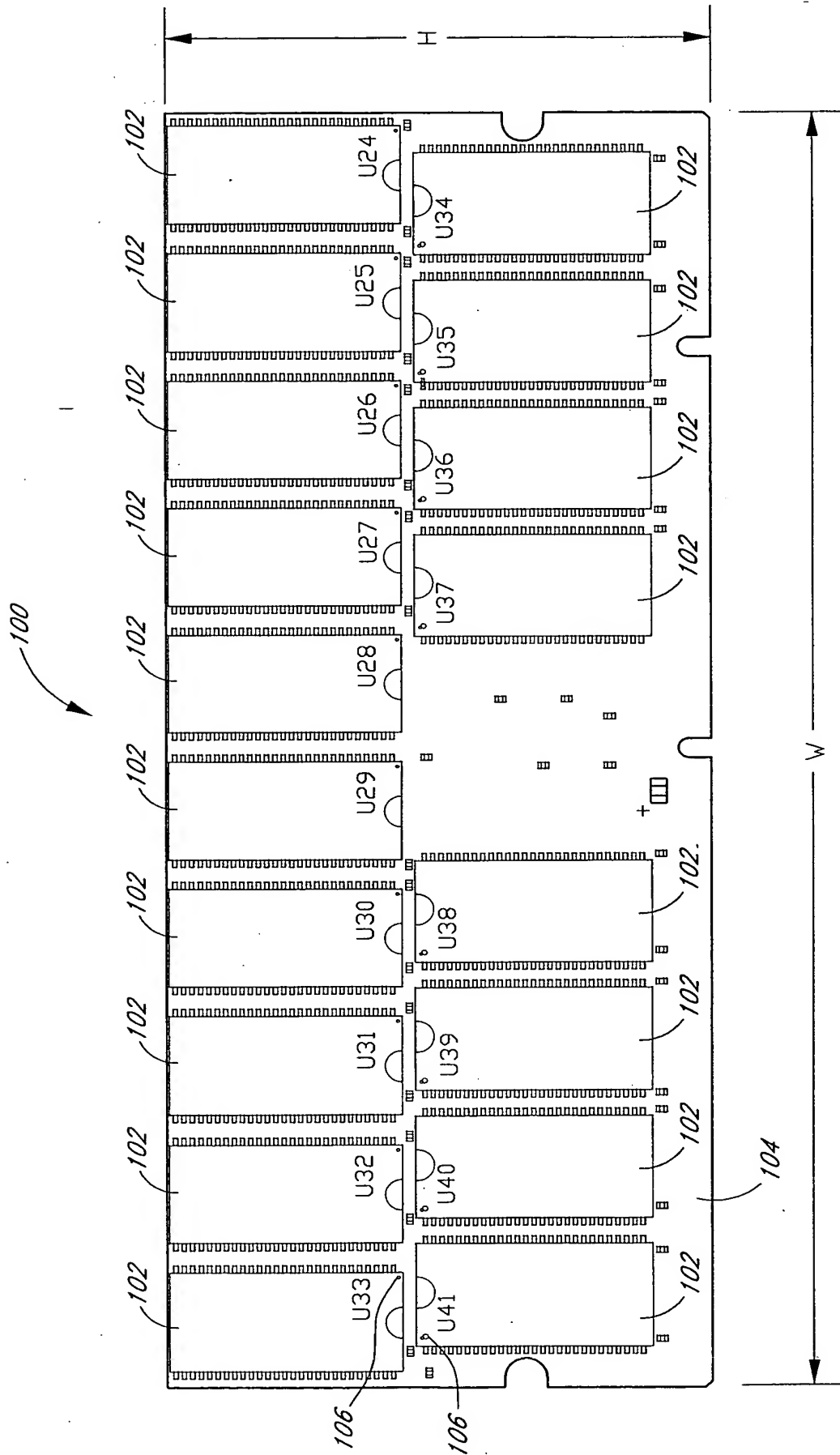


FIG. 1B

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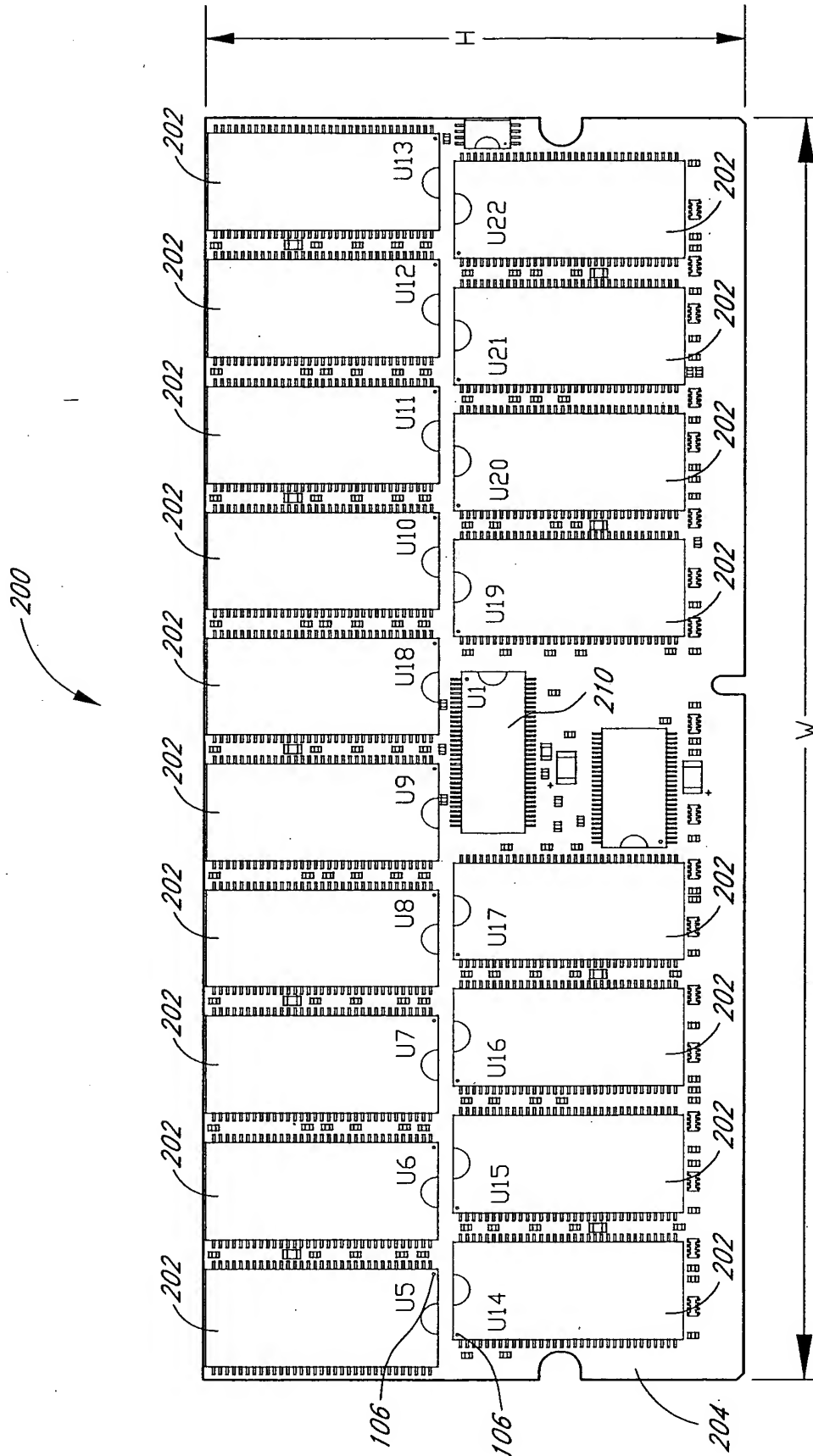


FIG. 2A

ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY
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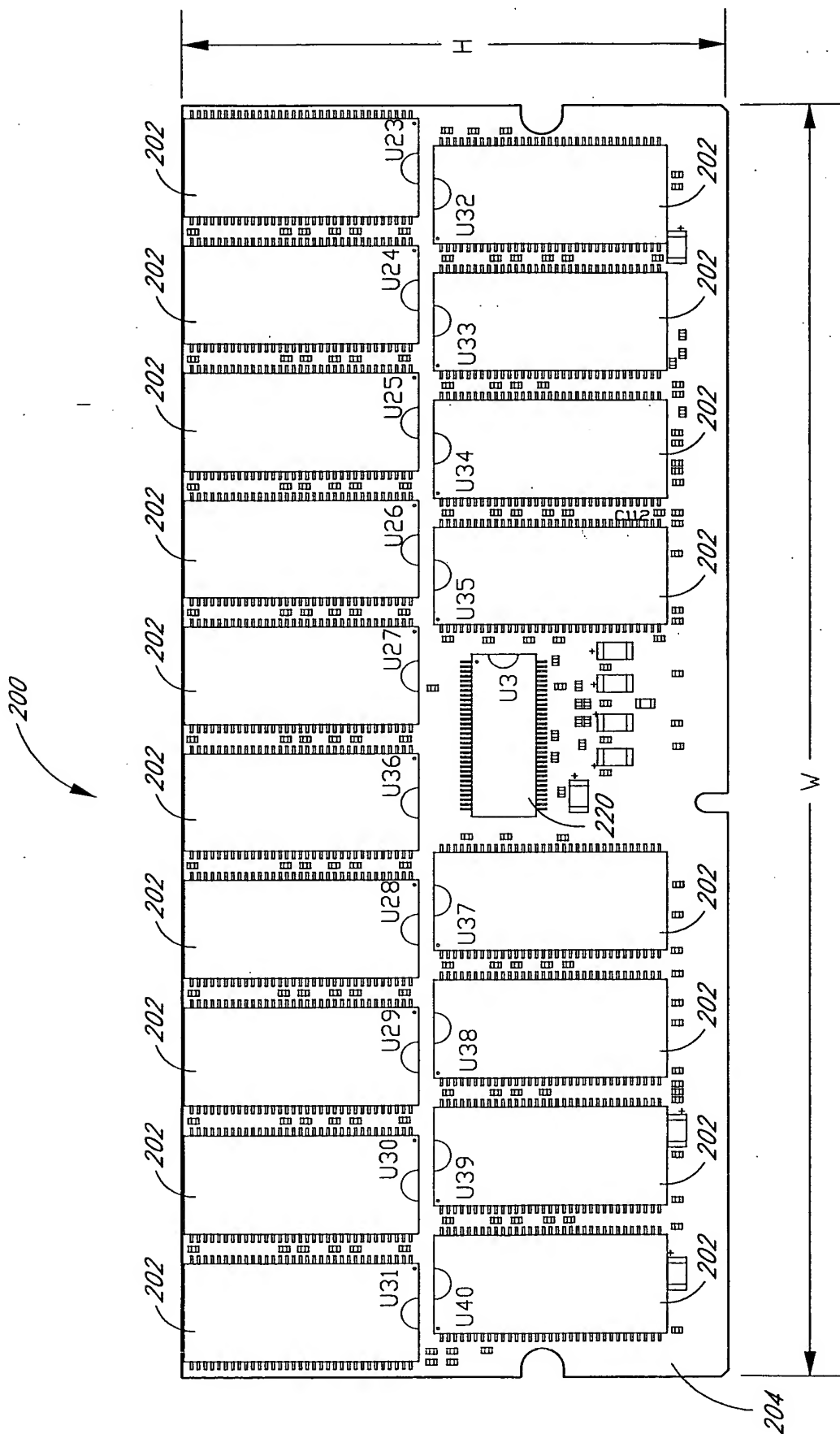


FIG. 2B

ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY
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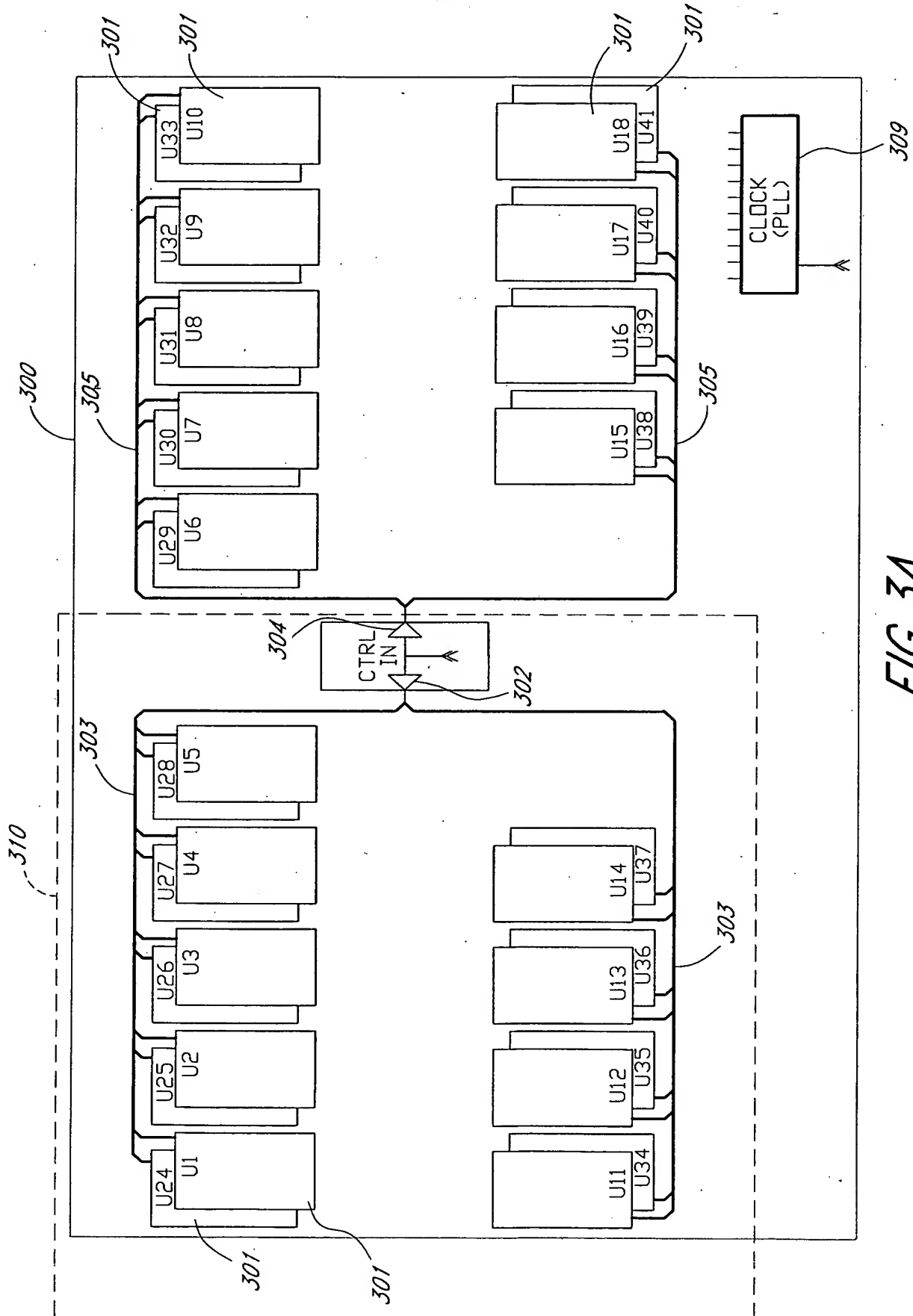


FIG. 3A

ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY MODULE

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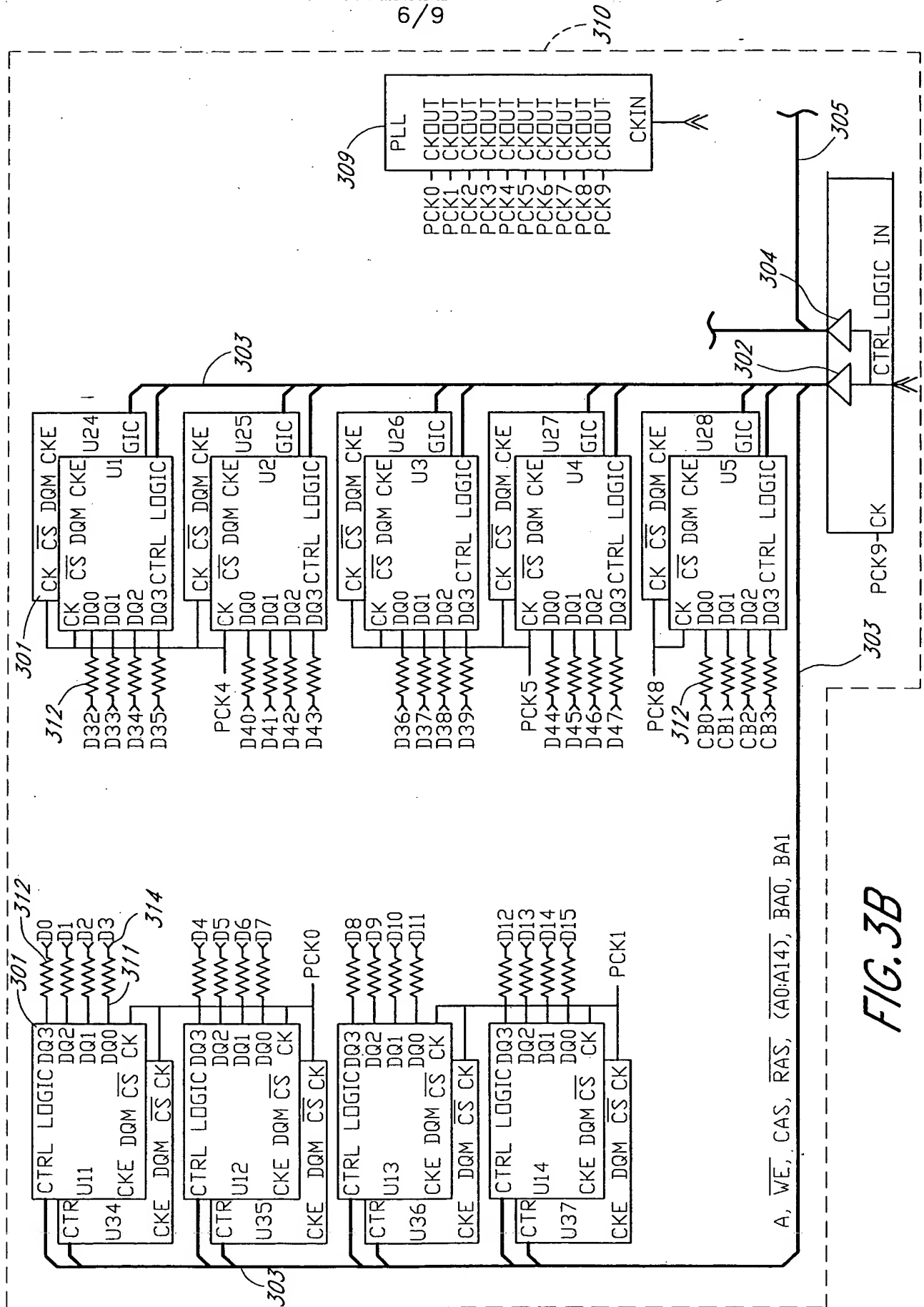
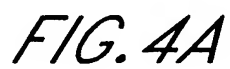


FIG. 3B

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ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY
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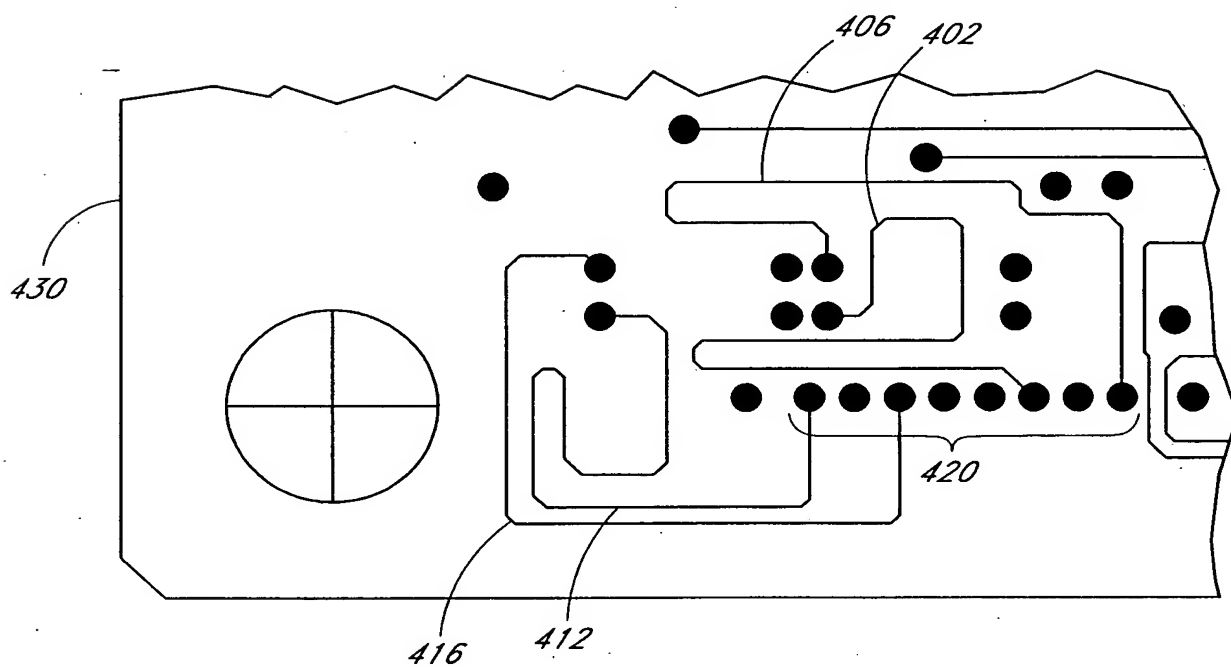


FIG. 4B

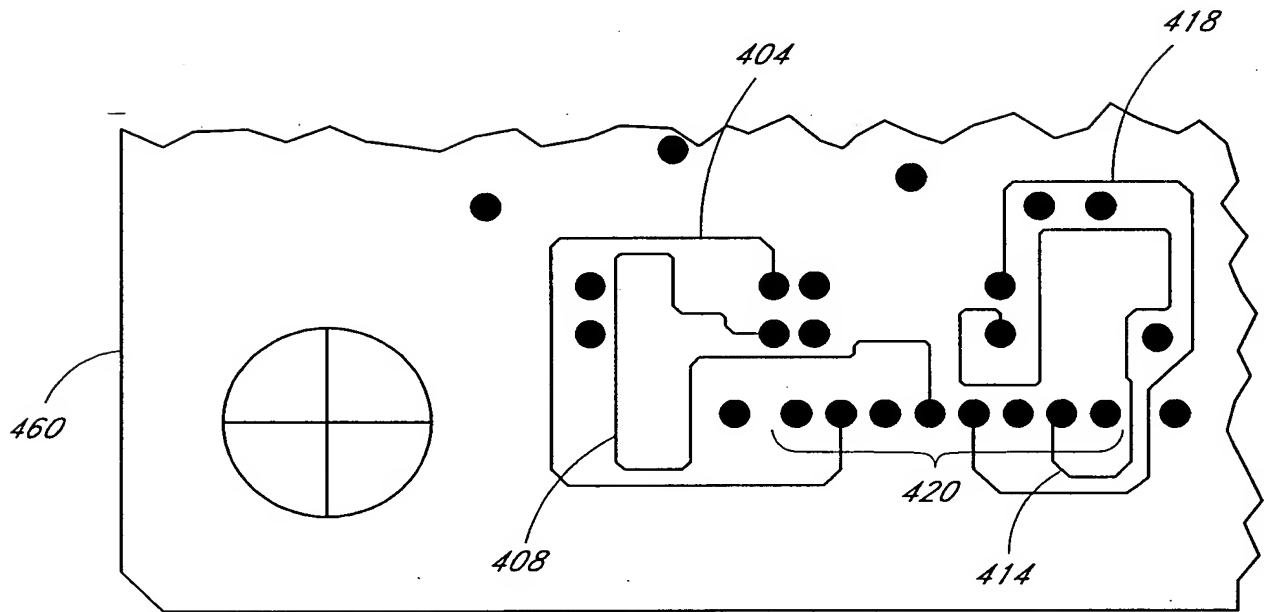


FIG. 4C

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